What is claimed is:

1. A MOSgated accumulation channel field effect transistor comprising a highly conductive silicon substrate of one of the conductivity types; a drift region of said one of the conductivity types disposed above said substrate; a channel region of said one of the conductivity types disposed above said drift region and having an impurity concentration less than that of said substrate; a plurality of trenches extending through said channel regions and into said drift region; each of said trenches having respective gate oxide liners along their vertical walls, and insulation liners at the bottoms of said trenches; a gate of the other conductivity type filling the interior of each of said trenches; an insulation cap over the tops of each of said gates in each of said trenches; a highly conductive source region disposed at the tops of the mesas between each of said trenches and above said channel regions which are in the mesas between each of said trenches; a Schottky barrier contact area formed in the top of each of said mesas; and a top contact metal connected to both said source regions and to said Schottky barrier contact areas.

2. The transistor of claim 1, wherein said one of the contact types is the N type.

3. The transistor of claim 1, wherein a Schottky barrier contact layer is disposed on said Schottky barrier contact area and is contacted by said top contact metal.

4. The transistor of claim 3, wherein said Schottky barrier contact layer is aluminum.

5. The transistor of claim 3, wherein said one of the contact types is the N type.

6. The transistor of claim 4, wherein said one of the contact types is the N type.

7. The transistor of claim 1, which includes a second plurality of trenches formed in at least selected ones of said mesas and spaced from the walls of said trenches forming said mesas; said Schottky barrier contact areas being formed in respective ones of said second plurality of trenches.

8. The transistor of claim 2, which includes a second plurality of trenches formed in at least selected ones of said mesas and spaced from the walls of said trenches forming said mesas; said Schottky barrier contact areas being formed in respective ones of said second plurality of trenches.

9. The transistor of claim 3, which includes a second plurality of trenches formed in at least selected ones of said mesas and spaced from the walls of said trenches forming said mesas; said Schottky barrier contact areas being formed in respective ones of said second plurality of trenches.

10. The transistor of claim 4, which includes a second plurality of trenches formed in at least selected ones of said mesas and spaced from the walls of said trenches forming said mesas; said Schottky barrier contact areas being formed in respective ones of said second plurality of trenches.

11. The transistor of claim 5, which includes a second plurality of trenches formed in at least selected ones of said mesas and spaced from the walls of said trenches forming said mesas; said Schottky barrier contact areas being formed in respective ones of said second plurality of trenches.

12. The transistor of claim 6, which includes a second plurality of trenches formed in at least selected ones of said mesas and spaced from the walls of said trenches forming said mesas; said Schottky barrier contact areas being formed in respective ones of said second plurality of trenches.

13. The device of claim 1, which further includes first and second gate contacts for said gates filling said trenches; said first gate contact connected to a first set of said gates; said second gate connected to a second set of said gates.

14. The transistor of claim 13, which includes a second plurality of trenches formed in at least selected ones of said mesas and spaced from the walls of said trenches forming said mesas; said Schottky barrier contact areas being formed in respective ones of said second plurality of trenches.

15. The device of claim 2, wherein said gates are formed of P type polysilicon.

16. The device of claim 6, wherein said gates are formed of P type polysilicon.

17. The transistor of claim 16, which includes a second plurality of trenches formed in at least selected ones of said mesas and spaced from the walls of said trenches forming said mesas; said Schottky barrier contact areas being formed in respective ones of said second plurality of trenches.

18. The process of forming a P type gate in a trench in a silicon wafer; said process comprising the steps of etching a trench in the surface of a silicon wafer to a given depth; forming a thin dielectric layer on the walls and bottoms of said trench; forming a relativity thin polysilicon layer on the walls of said trench without

completely filling said trench and thereafter implanting said thin polysilicon layer with an implant of a given species and thereafter filling the remainder of the interior of said trench; and thereafter activating said implant to cause the implant species to move into the main volume of polysilicon filling said trench.

19. In a MOSgated accumulation channel field effect transistor having a plurality of mesas separated by parallel gate-filled trenches; the tops of said mesas having a central Schottky barrier-receiving trench of relatively high resistivity surface flanked by source regions of relatively high resistivity surface; and a top contact connected to said source region surface with an ohmic contact and to said Schottky barrier receiving trench surface with a Schottky contact.

20. The transistor of claim 19, wherein Schottky barrier receiving trench is lined with a Schottky barrier material.

21. The transistor of claim 20 wherein the Schottky barrier material is aluminum.